EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 2001338987
PUBLICATION DATE : 07-12-01

APPLICATION DATE : 26-05-00
APPLICATION NUMBER : 2000157125

APPLICANT : NEC MICROSYSTEMS LTD;

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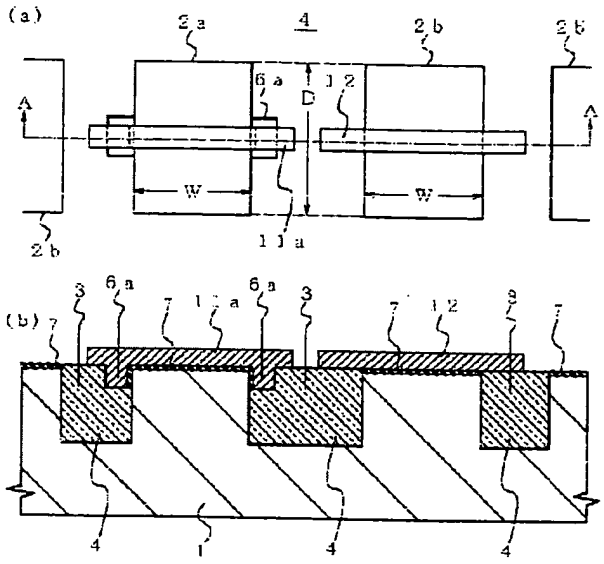
INT.CL. : H01L 21/8234 H01L 27/088 H01L 21/76 H01L 27/08 H01L 29/78

TITLE : FORMING METHOD OF SHALLOW TRENCH ISOLATION REGION OF MOS TRANSISTOR



ABSTRACT : PROBLEM TO BE SOLVED: To provide the forming method of STI easy to achieve high speed by suppressing the rapid increase of electric power consumption while suppressing the lowering of a latch-up tolerated dose without employing next generation alignment technology in a semiconductor device including a MOS transistor.

SOLUTION: A shallow trench 6a shallower than a shallow trench 3 is formed in the neighborhood of an element formation region 2a in STI comprising the shallow trench 3.